International Spillovers of Industrial Policy in the Global Semiconductor Sector

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October 2025

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Introduction: The Context

- Resurgence of Industrial Policy (IP) since 2021, not only in the US, but worldwide
- Economists generally skeptical towards IP because:
  - Breeds inefficiency (capture; informational problem)
  - In the international context: Potential for retaliation and race to the bottom
- But International Trade economists –> more nuanced attitude
  - Reason: Focus on International Spillovers. National sovereign governments are free to waste their own resources
  - International Spillovers of IP: Mostly positive –> lower prices for consumers in other countries
  - Attitude reflected in lack of clear IP/subsidy rules in the WTO

Introduction (contd.)

- Current State of Affairs at WTO:
  - Prohibited Subsidies (Export, Import Substitution –> Discriminatory)
  - Actionable (complaining country has to prove injury)
  - Notification Requirements - but not enforceable

- General View: Subsidy/IP not regulated - in contrast to tariffs, various NTBs
  - May have contributed to the backlash against multilaterism

Introduction (contd.)

- Attitude has changed recently - partly in response to rise of IP. What is different now?
  - Political Economy matters.
    - Firms and workers in other countries may be adversely affected (even if consumers gain)
  - Production and Trade are organized in GVCs
  - National Security concerns –> but will NOT go there
- Demand for New Policy Design
  - Should the WTO devise rules to regulate IP? And if so, how should these rules be designed?

Introduction (contd.)

- In this talk, will focus on semiconductors
- Focus on technological cross-border spillovers
- Work still in progress, but preliminary insights/working hypothesis:
- In the age of GVCs, IP not only has important cross-country spillovers, but such spillovers may be a prerequisite for successful IP.
- Sources of Cross-border Spillovers: Active area of research
- Evaluation of IP: Active area of research

Road Map for the Rest of the Talk

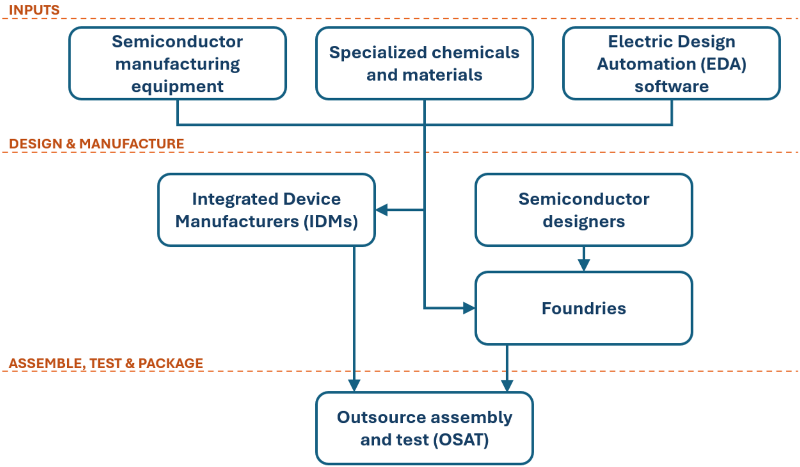
1. Why Semiconductors: A brief overview of global trends in the sector
2. Measurement
   - Measurement Challenges
   - Our Approach –> Combine three different approaches
   - Preliminary insights from first two approaches
3. A model-based approach with its pluses and minuses
4. Main results. Implications for cross-border effects
5. Current research:
   - Identifying mechanisms behind cross-border learning
   - Assess the effects of IP through counterfactual simulations
6. Tentative Conclusions/Insights

1. Why Semiconductors

- Semiconductors widely perceived as a strategic industry
  - Driver of economic growth: backbone of the modern economy, R&D intensive
  - Dual-use: national security motivations
- "Scattered" evidence that industry receives vast amounts of government support
- Anecdotally, learning-by-doing (LBD) and dynamic comparative advantage often invoked to justify infant industry promotion
- But no rigrous evidence on these issues since Irwin and Klenow (1994) who focused on memory chips. Industry has changed significantly since then.

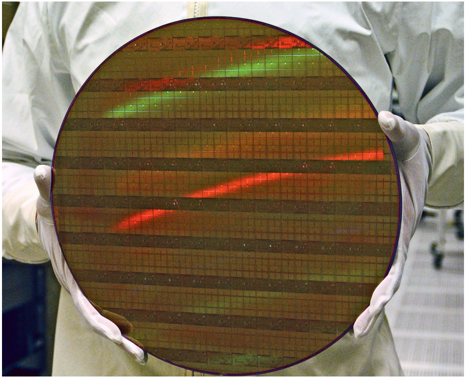
The semiconductor value chain

A highly fragmented and globalized industry, with large concentration at specific stages of production. ▸ Examples



Simplified version of Bown (2020)

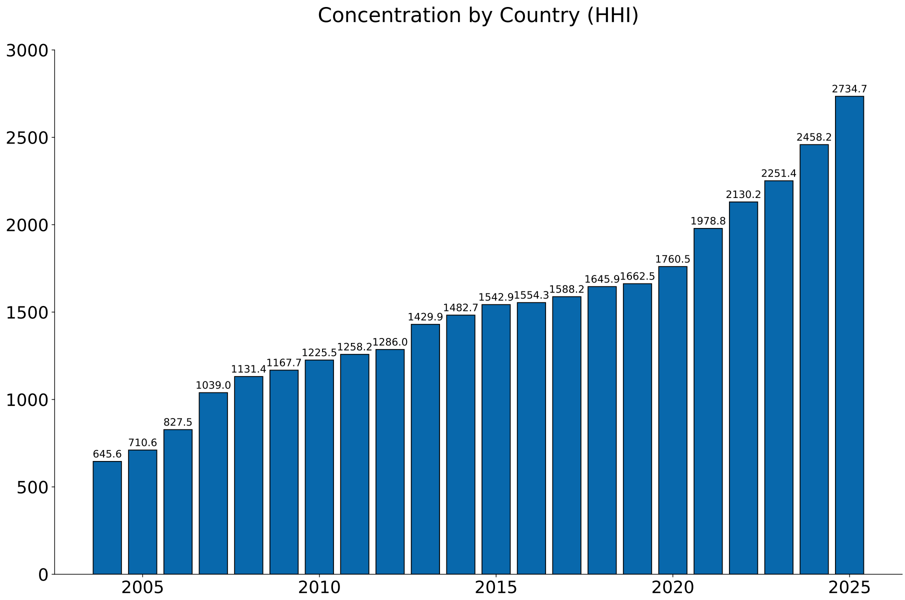
Two Types of Firms in the Second Layer



Intel 300 mm wafer with 45 nm Core 2 Duo Wolfdale Chips (2007).

- Integrated Device Manufacturers (IDMs) own their fabrication facility.
  e.g., Intel, Texas Instruments
- "Fabless" firms outsource production to third-party foundries.
  e.g., AMD, Nvidia, Qualcomm
- 20% of firms are IDMs, 80% are Fabless.

The industry is concentrated geographically.



With particularly high concentration at specific parts of the supply chain.

- ASML and TSMC have over 90% market share at specific segments

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How ASML became chipmaking's biggest monopoly

A low-key Dutch company has cornered a critical link in the global electronics supply chain

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TSMC's Dominance Is Starting to Worry More Than Just Rivals

The TSMC campus in Hsinchu, Taiwan. *Photographer: An Rong Xu/Bloomberg*

- And these are the best known examples

Taiwan Semiconductor Manufacturing Company (TSMC)

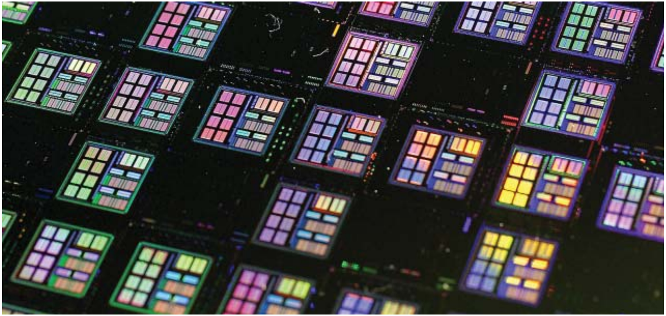
The Economist

Subscribe   Welcome

Shifting silicon

TSMC is about to become the world's most advanced chipmaker

Intel is pushed into second place by a Taiwanese rival

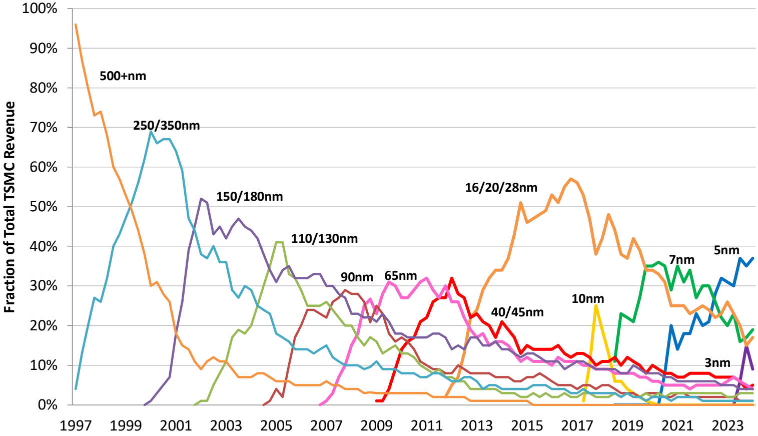


Taiwan Semiconductor Manufacturing Company (TSMC)

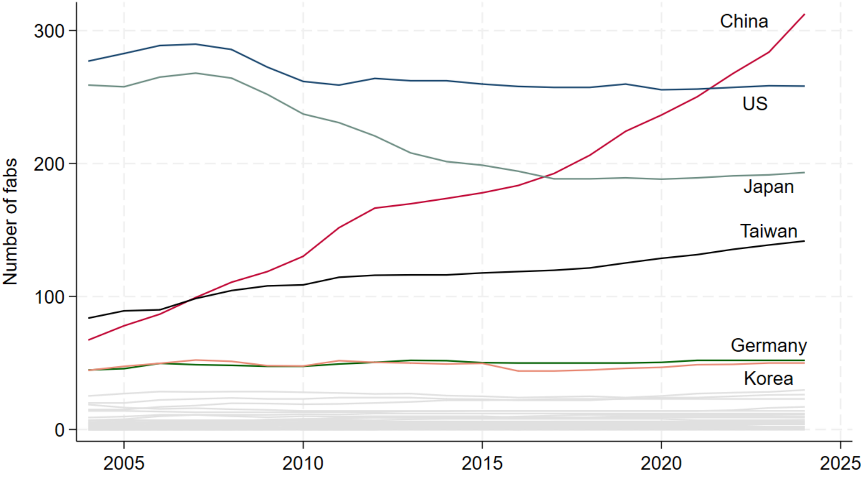
- Founded in 1987 by Morris Chang after recruitment by the Taiwanese government.
  - *Former head of semiconductor business operations at Texas Instruments.*
- Government sought to boost the country's high-tech sector in order to compete with firms in Japan and the United States.
  - *Reminiscent of recent efforts by the Chinese government's to develop its own semiconductor industry.*
- Taiwan's comparative advantage:
  1. Educated population,
  2. Low wages,
  3. Weak environmental regulations,
  4. Government financial and policy support.

Production cycles at TSMC

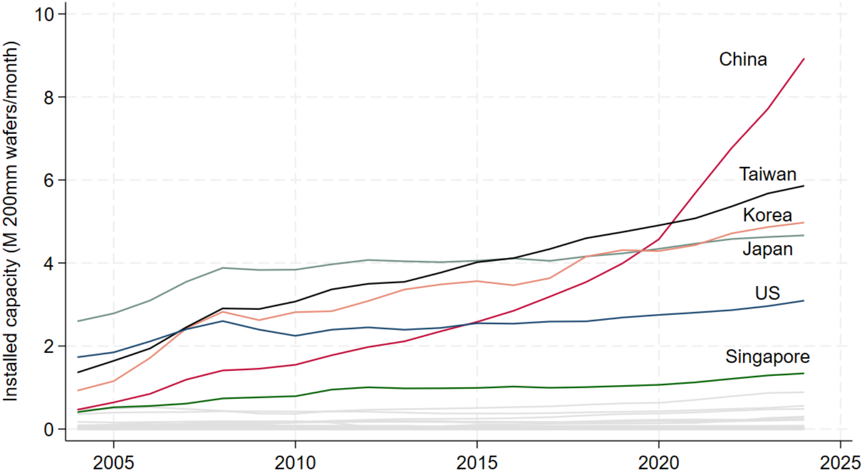
Rapid ramp up of new products, with multiple vintages in production at any given time.



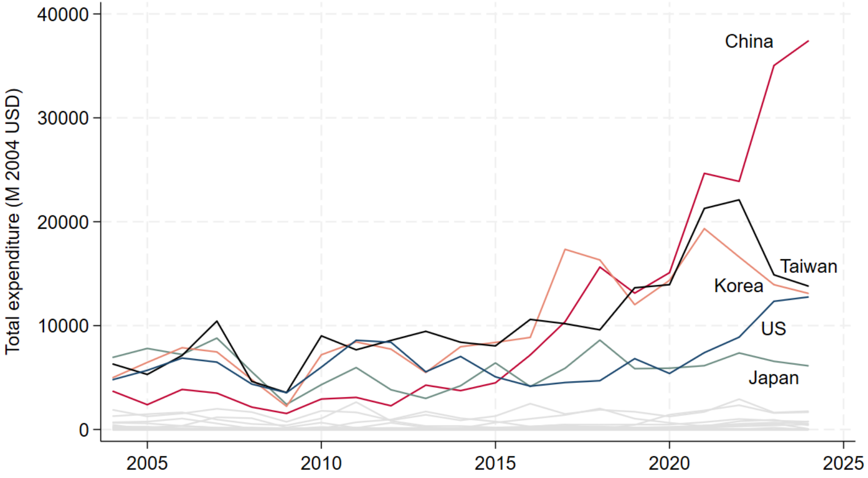
China has Increased its Fabs...



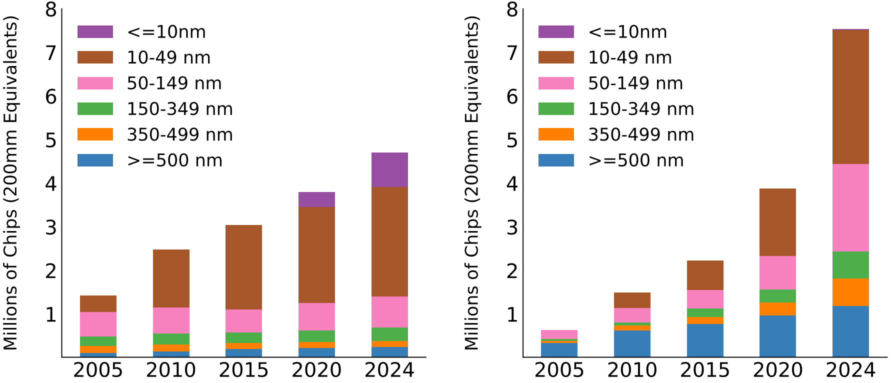
and its Capacity (200 mm equivalents) ...



But this Growth is Expensive



China has not caught up (yet) in frontier technologies



(a) Taiwan (Leader)

(b) China (Follower)

Learning-by-doing in semiconductors

- Modern manufacturing of semiconductors requires unprecedented precision.
- Scope for LBD through:
  - Hands-on experience and innovation on production floor.
  - Close collaboration with buyers and input suppliers –> Learning along the Supply Chain

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- But LBD where?
  - Within a firm-technology pair?

    Conventional wisdom and Irwin and Klenow (1994) support this view
  - Within firm, across technologies (economies of scope)?
  - Across firms?

    Collaborations along supply chain could spill over to other firms.

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$\implies$ Different implications for desirability of IP: Need to estimate empirically.

2. Measurement

- Measurement Challenges
  - Grants vs. other forms of support
  - Prevalence of below market financing in China
  - Difference between ex-ante and ex-post measures
  - Difference between stock and flow of IP
  - Implementation differences across countries (see China in particular)

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- Our Approach: Combine three approaches
  - Historical analysis
  - Machine learning on government documents (JLOP 2023)
  - Model-based approach

Approach 1: Historical Industrial Policy

- LBD & dynamic comparative advantage suggests optimal policy is complicated and requires a long view.
- All major players in the industry today used aggressive industrial policy, particularly when the industry was in its infancy.
- Common themes:
  1. Generous financial support, government often took the lead.
  2. Foreign tech transfer via joint ventures, outward FDI, tech licensing, etc.
- Some evidence that China has not succeeded in reaching the frontier because it had 1, but not enough of 2 (c.f. Minnich 2023)

Approach 2: Measuring government support in the industry today

Use Juhasz et al. (JLOP) 2023 to identify and quantify semiconductor industrial policies in the Global Trade Alert (GTA) for 2010-2022:

Identify - Use HS codes and Natural Language Processing (NLP) to select semiconductors policies from total IP dataset (JLOP)

Quantify - Assign quantities (dollar values) to each semiconductor policy using source documents

Validate - Observations are validated using area-specific RAs.

Evaluating our Approach

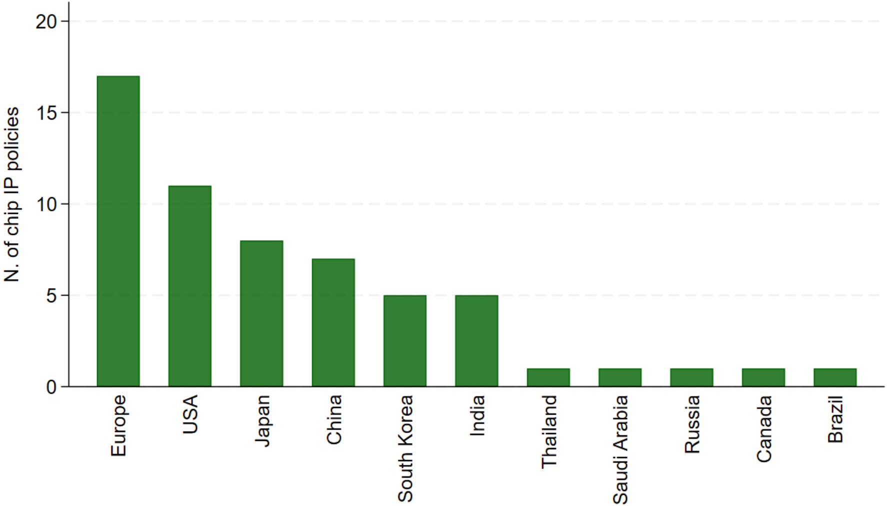
- Advantage: Ex-ante measure of what the state is trying to do
- Challenge: Count-based measure mixes major national policy announcements and disbursements of support to individual firms
  - We quantify spending based on announced financial support
  - We show results dropping policies targeted towards individual firms
- Problem: This method for quantifying spending does not work for China
  - Supplement China's value from *JW Insights* (via *Financial Times*)

Overview of results

Given the measurement challenges, we present results three ways

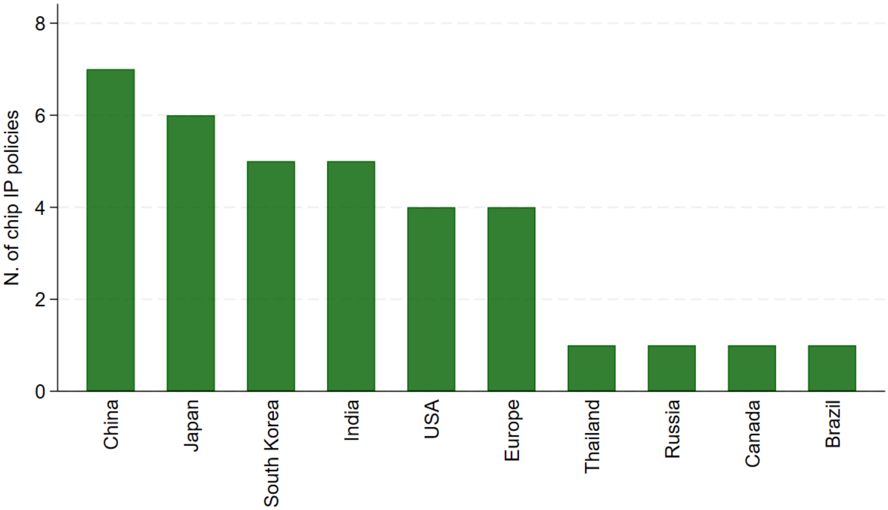
1. Count of all policies by implementing country
2. Count of national policies (excludes disbursements to individual firms)
3. Value of fiscal support

Count total policies



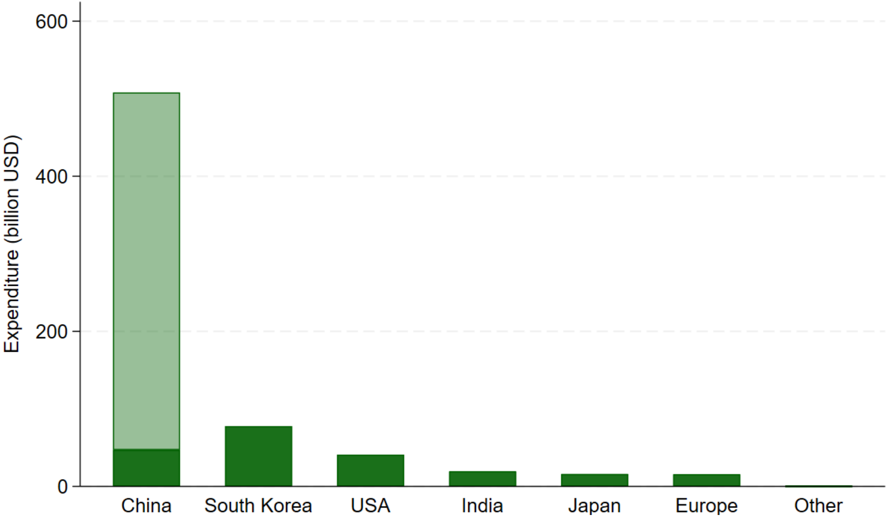
IP is concentrated ($n = 17$): current major producers + India
Taiwan the only major producer for whom we don't identify any IP

Count national policies only



USA and European countries have many policies targeting individual firms.

Support by country – dollar values



Chinese IP substantial, but not an outlier based on market size.

Additional findings

- Increase in policy activism from 2020 (Korea, Japan, US, Europe.) ▸ IP Time Trend

- All parts of the supply chain receive support but most policies target "Design and Manufacture."

- Stated intent is typically economic growth and enhanced competitiveness.

- Subsidies are the dominant form of support.

$\implies$ Features motivate our modeling choices: focus on foundries and subsidies. For now, only production subsidies due to data limitations.

Main Insights from this Analysis

- Every country has heavily subsidized semiconductors, especially early in the industry's development
- China does not appear to be an outlier, especially if one scales by GDP or population
- Some countries no longer subsidize (e.g, Taiwan). Speaks to stock vs. flow distinction, and importance of dynamic comparative advantage

Main Insights from this Analysis

- Every country has heavily subsidized semiconductors, especially early in the industry's development
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- Some countries no longer subsidize (e.g, Taiwan). Speaks to stock vs. flow distinction, and importance of dynamic comparative advantage
- Most important: No industry development in follower countries without acesss to foreign frontier technology.
  - Hypothesis: IP is only successful when paired with access to frontier (foreign) technology

3. A Model-Based Approach

Demand

- Each period t, buyers maximize a nested CES objective function over technologies k and suppliers j:

$$Q_t = \left[\sum_{k \in K} \zeta_{kt} \, q_{kt}^{\frac{\eta-1}{\eta}} \right]^{\frac{\eta}{\eta-1}}$$

  where

$$q_{kt} = \left[\sum_{j \in J} \left(\xi_{jkt} \, y_{jkt} \right)^{\frac{\sigma-1}{\sigma}} \right]^{\frac{\sigma}{\sigma-1}}$$

  and $\sigma > \eta > 1$, meaning that chips within a technology are more substitutable than chips across technologies.

- Buyers are static utility maximizers.

Demand

- Buyer preferences vary over varieties (ξ_{jkt}) by source, technology, and time:

$$\xi_{jkt} = \bar{z}_{jkt}^{\delta} \times \nu_j^D \times \phi_k^D \times \rho_t^D \times \Delta\xi_{jkt}$$

  where $\bar{z}_{jkt}$ denotes a "quality index" constructed on the basis of observable characteristics X_{jkt} ▸ Quality Index

- Yields demand from supplier j conditional on technology k:

$$\begin{aligned}\log(y_{jkt}) = & -\sigma \log(p_{jkt}) + (\sigma\delta)\log(\bar{z}_{jkt}) + \underbrace{(\sigma)\log(\nu_j^D)}_{\text{Country FEs}} \\ & + \underbrace{(\sigma)\log(\phi_k^D)}_{\text{Technology FEs}} + \underbrace{(\sigma)\log(\rho_t^D)}_{\text{Time FEs}} \\ & + \underbrace{\log(R_{kt}P_{kt}^{\sigma-1})}_{\text{Technology/Time FEs}} + \underbrace{(\sigma)\log(\Delta\xi_{jkt})}_{\text{Idiosyncratic shocks } (\varepsilon_{jkt})}\end{aligned}$$

Demand

- Similarly, demand for technology k is given by:

$$\log(q_{kt}) = -\eta \log(P_{kt}) + \underbrace{\eta log(P_t) + \log(Q_t)}_{\text{Time FEs}} - log(\zeta_{kt})$$

where:

and $P_{kt} = \left[\sum_j \left(\frac{p_{jkt}}{\xi_{jkt}} \right)^{1-\sigma} \right]^{\frac{1}{1-\sigma}}$ is the CES price index for technology k

and $P_t = \left[\sum_k \zeta_{kt}^{1-\eta} \; q_{kt}^{1-\eta} \right]^{\frac{1}{1-\eta}}$ is the CES price index in quarter t.

Supply

- Each source country j is operated by a single firm
  - TSMC in the case of Taiwan
  - SMIC in the case of China

- Firm j maximizes expected discounted profits using quantities (or prices) as the strategic variable. For quantity competition:

$$\max_{\{y_{jkt}\}} \left\{ E_0 \sum_{t=0}^{\infty} \left[\left(\frac{1}{1+d} \right)^t \sum_{k \in K} \left(p_{jkt}(y) y_{jkt} - c_{jkt}(y) y_{jkt} \right) \right] \right\}$$

Learning-by-Doing

- Assume costs are

$$\log\left(c_{jkt}\right) = \gamma \log\left(H_{jkt}\right) + \kappa \log(\bar{z}_{jkt}) + \zeta \log(w_{jt}) + \log\left(\nu_j^S\right) + \log\left(\phi_k^S\right) + \log\left(\rho_t^S\right) + u_{jkt} .$$

  where H is the firm's stock of knowledge and w_{jt} are country-time manufacturing wages.

- Learning-by-Doing exists when $\gamma \leq 0$.
- We follow Irwin and Klenow (1994, JPE) and model learning-by-doing as follows:

$$H_{jkt} = 1 + \underbrace{Y_{jkt}}_{\text{Technology}} + \underbrace{\alpha \times (Y_{jt} - Y_{jkt})}_{\text{Intra-Firm}} + \underbrace{\mu \times (Y_{Wkt} - Y_{jkt})}_{\text{Across Firms}}$$

- Firms can learn because of improvements within technology, across technologies but within firm, and across firms.

Optimal Pricing

- Firm chooses price as a markup over dynamic marginal cost.

$$p_{jkt} = \frac{\varepsilon(s_{jkt})}{\varepsilon(s_{jkt}) - 1}\left(c_{jkt} + \overbrace{\frac{\gamma}{1+d} \times E_t\left[\sum_{r \in K} \frac{\Delta_{r,k} c_{r,t+1} y_{r,t+1}}{H_{r,t+1}}\right]}^{\text{Dynamic Incentive}}\right)$$

$$\text{where } \Delta_{r,k} \equiv \begin{cases} 1-\mu & \text{if } r = k \\ \alpha - \mu & \text{if } r \neq k \end{cases}$$

- LBD makes the cost dynamic so the firm internalizes future cost reductions conditional on period t information.
  - This is Boston Consulting's famous "Experience Curve."
- Comparative Statics:
  - Price falls when $\gamma < 0$ and $\alpha > 0$.
  - Price increases when $\mu > 0$ (free-riding)
  - Price decreases when $\gamma < 0$ and $E[y_{t+1}] > 0$.

Optimal Pricing (contd.)

This formulation can accommodate several supply-side models:

- **Quantity Competition**: $\varepsilon(s_{jkt}) = \left[\frac{1}{\sigma}(1 - s_{jkt}) + \frac{1}{\eta} s_{jkt}\right]^{-1}$
- **Price Competition**: $\varepsilon(s_{jkt}) = \sigma(1 - s_{jkt}) + \eta s_{jkt}$
- **Monopolistic Competition**: $\sigma = \eta; \varepsilon = \sigma; Markup = \frac{\sigma}{\sigma - 1}$
- **Cournot** (homogeneous products within technology k): $\varepsilon(s_{jkt}) = \frac{\eta}{s_{jkt}}$

Results in the tables today based on Quantity Competition.

Do Foundries Internalize LBD?

TSMC Margins

From Interview with Morris Chang (on SEMI Website):

- *And then I went to integrated circuits, became the general manager of integrated circuits and there we started a learning curve, a methodical use of the learning curve... as a control, as an influence on pricing and as it influences our cost reduction efforts. This was a pioneer effort in the semiconductor industry. We did it together with the Boston Consulting Group... This was in the late 60s... And we used what we worked out with loads of data, a lot of theory and a lot of effort put into the practice of the theory and use of the data we had already taken. The result was so called learning curve pricing. And we would automatically reduce the price every quarter, even when the market did not demand lower price. And this was a very successful effort even though it was somewhat controversial. A lot of people thought that we were being foolish. Why do you reduce price when you did not have to? But we did that because I believed in it and indeed our market share just kept expanding.*

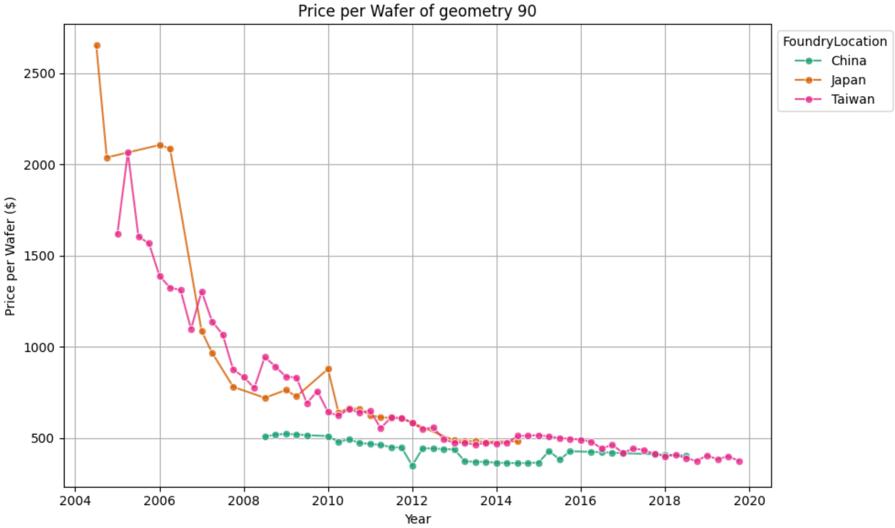
And from TSMC's Earnings Calls:

- "We expect to have a very fast and smooth N7 ramp-up in 2018, with its yield learning even better than our 16-nanometer."
- "This N7+ will ride on N7 learning to have a very steep yield learning curve."
- "We expect the in N7 to benefit greatly from N10 and our progress so far has been on schedule."

Data

- Wafer Pricing Survey (source: Global Semiconductor Alliance)
- Buyers provide GSA information for each of their orders in a given quarter.
  - The quid-pro-quo is that GSA provides survey respondents with benchmarking data.
- Detailed pricing information of Foundry pricing to Fabless firms including price per wafer, characteristics, foundry location, Fabless location.
- Coverage: Quarterly, 2004 to 2019.

Learning-by-Doing in Wafer Prices?



Learning-by-Doing in Wafer Prices?

- Downward trends in prices in early years.
- Sourcing from Taiwan and Japan is more expensive than China.
- China enters with low prices. Downward trend in prices much less pronounced. But true for all latecomers. PriceTrends

Estimation: Demand

- Estimation of demand and supply via generalized method of moments (GMM) using the GSA panel data.
- GMM estimator block-diagonal: Demand estimates not afffected by supply structure.
- Demand-side Instruments: Country-specific wages and supplier-specific "experience".
- Fixed effects: Technology; Country; Time-Technology.
- Demand-side Elasticities:
  - $\eta = -2.7$
  - $\sigma = -6.4$ (OLS estimate: -2.6)
  - precisely estimated

Estimation: Supply

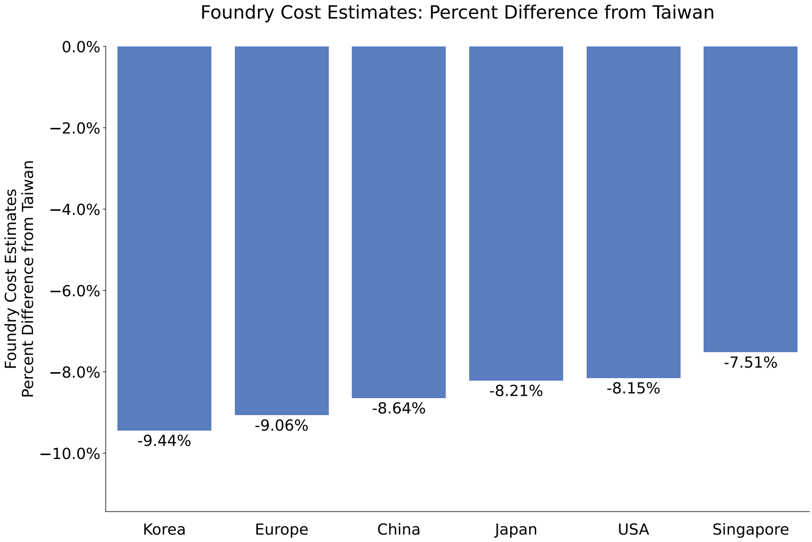
- Supply-side instruments: Period $t-1$ variables as instruments (structural errors orthogonal to firms' information sets).
- **Time fixed effects** control for global shocks to supply (*e.g.*, photolithography), global input prices (*e.g.*, silicon), technological progress.
- **Technology fixed effects** control for unobservable charactersitics affecting costs.
- **Manufacturing wages** collected from countries' statistical agencies control for labor cost differences.
- **Country fixed effects** control for unobserved cross-country cost differences (*e.g.*, subsidies).

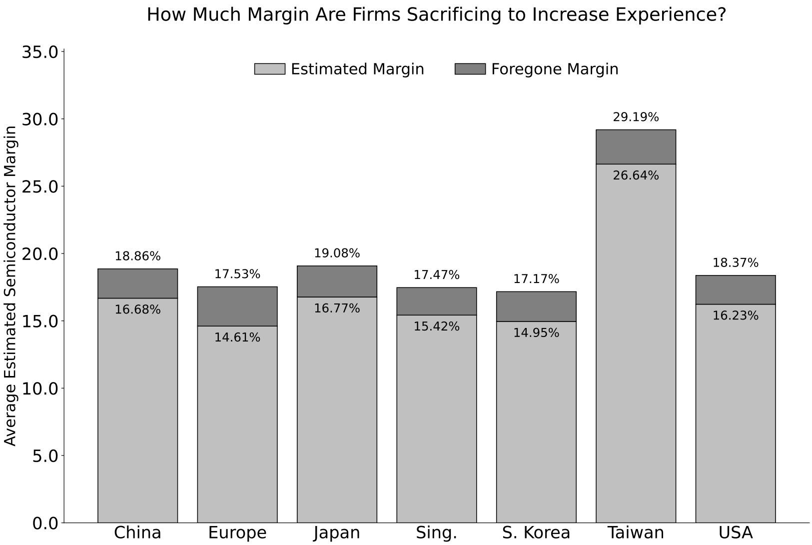
4. Main Results

- Costs increasing in wages.
- Supply-side country FEs consistent with our qualitative findings on subsidies.
- Precise estimates of Learning-by-Doing (with quarter fixed effects):

	(1)		(2)		(3)	
Parameter	Estimate	SE	Estimate	SE	Estimate	SE
Technology (γ)	-0.15	(0.01)	-0.18	(0.03)	-0.83	(0.25)
Firm (α)			0.01	(0.02)	0.23	(0.10)
World (μ)					0.05	(0.02)
Learning Rate	10%		12%		44%	
[95% CI]	[8%-11%]		[8%-15%]		[21%-60%]	

- Cross-border spillovers (μ) statistically significant.
  - *We hypothesize this leads governments to over-use subsidies.*


Foundry Cost Estimates: Percent Difference from Taiwan
Foundry Cost Estimates
Percent Difference from Taiwan
0.0%
−2.0%
−4.0%
−6.0%
−8.0%
−10.0%
-9.44%
-9.06%
-8.64%
-8.21%
-8.15%
-7.51%
Korea
Europe
China
Japan
USA
Singapore



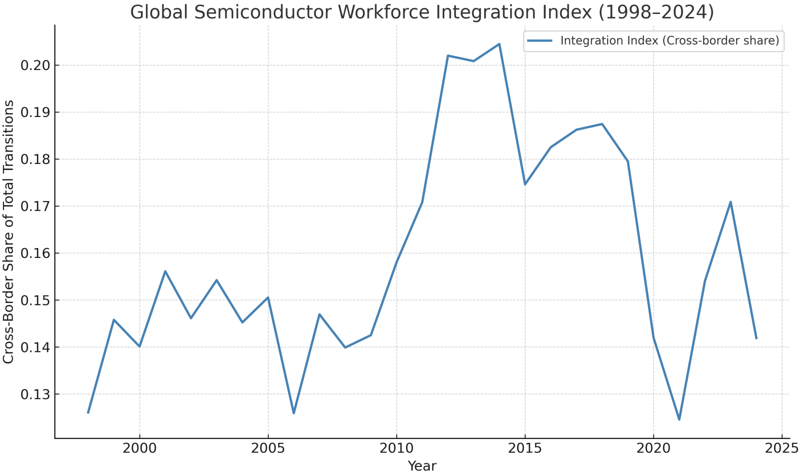
How Much Margin Are Firms Sacrificing to Increase Experience?
Estimated Margin
Foregone Margin
Average Estimated Semiconductor Margin
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
18.86%
16.68%
17.53%
14.61%
19.08%
16.77%
17.47%
15.42%
17.17%
14.95%
29.19%
26.64%
18.37%
16.23%
China
Europe
Japan
Sing.
S. Korea
Taiwan
USA

5. Sources of Cross-Border Learning Spillovers

- Focus of current research project

- Possible Sources:
  1. Identification Challenge: Perhaps Global Spillovers reflect Subsidies early in the product cycle?
  2. Labor Mobility / Poaching of Professionals and Experts
  3. Technology-node specific Patents
  4. Joint Ventures; FDI (both inward and outward)
  5. Access to Imports of Specialized Inputs (Capital Equipment, Software)
  6. Nature of Global Supply Network in Semiconductors:
     –> Highly Fragmented, yet Concentrated
     - Importance of Firm-to-Firm Relationships (WDR 2020)
     - Example: TSMC works closely with ASML to optimize ASML's equipment and software for the next technology node –> learning by TSMC AND ASML. ASML later works with SMIC who benefits from this learning.

On International Labor Mobility



On Learning along the Supply Chain

- Evidence of working out technological problems together with input suppliers

  From TSMC's earnings calls 2014-2017 as EUV technology is being developed:

  - "We work very closely with ASML and however it's not without the challenges. And we made a very good progress on the source power as well as on the photo resist. And for mass inspection solution it appears more likely. However, the current technology's challenge is more on the mask of the EUV technologies. That is currently actively working with ASML."
  - "Both our EUV tool development and the lithography process development have progressed very well in the past six months. We have worked closely with our tool partner, ASML(...)."

Learning along the Supply Chain (contd.)

- Evidence for R&D collaboration with customers

  From TSMC's earnings calls:

  - "TSMC has been working with customers to develop technologies required for IoT products such as sensors and various mainly low power devices."
  - "We recently see TSMC hang up with NVIDIA, Synopsys and ASML on 2-nanometer production and beyond."

Learning along the Supply Chain (contd.)

- Close collaboration in R&D
  - Among competitors, along the supply-chain
  - Example: Samsung, TSMC and Intel worked with ASML on EUV technology
    - During the 2010s, the three companies had a 25% stake in ASML and contributed to R&D funding
    - “We welcome Intel as the first customer to agree to contribute to these investments, the results of which will be available to every semiconductor manufacturer with no restrictions” (from earnings calls)

Next Steps

- Continue the investigation of spillover sources
- Assess the effects of IP through counterfactual simulations
  - Effects of unilateral policies on own country output and profits
  - Effects of unilateral policies on other countries' output and profit
  - Effects of "subsidy race"
- Interesting Hypothesis: In the presence of positive cross-border learning effects, IPs could be global complements

6. Tentative Conclusions/Insights

- IP widespread, both historically and today.
  - No "follower" country has developed its semiconductor sector without access to foreign frontier technology
  - IP appears necessary but *not* sufficient condition for success –> could explain China's technological lag
  - China deploys substantial IP, but is not an outlier, and is still not at the frontier.

- Large cross-border spillovers suggest the scope for subsidies as global complements.
  - These could be (at least in part) the outcomes of voluntary actions (FDI, tech transfer, etc).
  - *With* access to foreign frontier technology, catch-up by laggards is possible
  - Policy tools could be used to prevent rival countries from reaching the frontier.

Backup slides

Creating Helpful Incentives to Produce Semiconductors (CHIPS)

Return

- Signed into law on August 9, 2022.
- Motivated by disruptions in various industries (automotive, electronics, etc.) and highlighted vulnerabilities in supply chains.
- Large manufacturing concentration in Taiwan which also raises national security concerns.
  - Dependency on foreign suppliers.
  - Risks to critical infrastructure.
- GenAI (*e.g.*, ChatGPT) has industry and governments positioning to lead a "fifth industrial age."
- **Funding:**
  - $52 billion allocated for semiconductor research, development, and manufacturing.
  - $39 billion in manufacturing incentives.
  - $13 billion for R&D and workforce development.

Examples

Semiconductor Products	Example Firms	Example End-Products
1. Microprocessors	AMD, Intel	Computers, servers
2. "System on a Chip"	Broadcom, Nvidia, Qualcomm	Mobile phones
3. Commodity integrated circuits	Analog Devices, Xilinx	Barcode scanners
4. Memory	IBM, Samsung, Toshiba	Computers, flash drives

Contrasting our approach with OECD (2019)

	OECD (2019)	This paper
Aim	Quantify market distortions	Identify industrial policies
Years covered	Average for 2014-2018	2010-2022
Unit of analysis	Firms	Policies
Support reported for	21 firms	Countries
Input data	Companies' own publications and financial disclosures	JLOP (2023) for classifying industrial policies in GTA

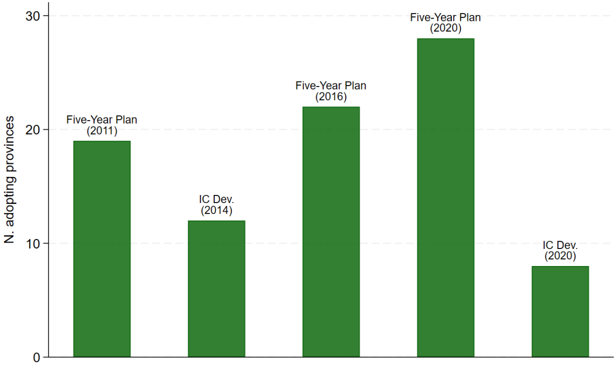
Back

Contrasting our approach with OECD (2019)

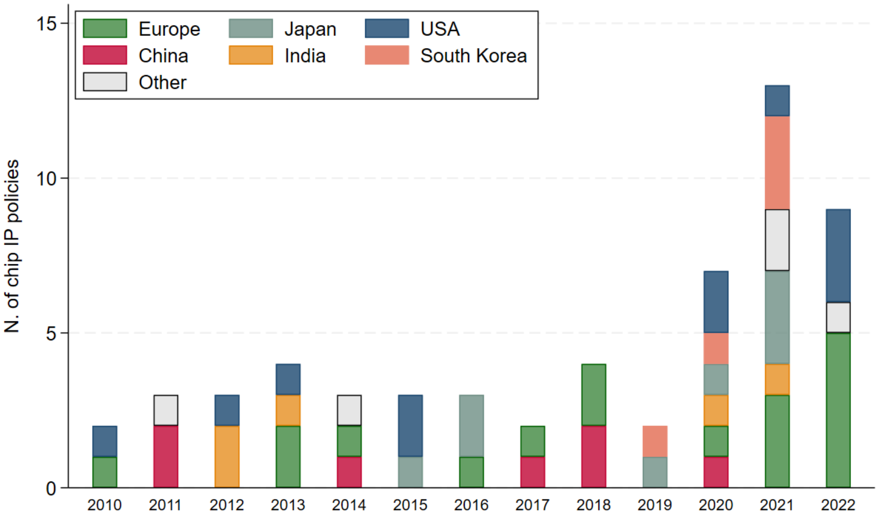
- Approach is conceptually different to the OECD report:
  - Builds from the “bottom up” and quantifies support at the level of the firm (not country)
  - Captures budgetary financial support and below market financing
- OECD advantages: inherently suited to quantifying support
- OECD disadvantages:
  - Relies on some strong assumptions: IP changes incentives for firms on the margin
  - Biased towards large, successful firms

◂ Back

Chinese provincial adoption



Support by country over time (all policies)



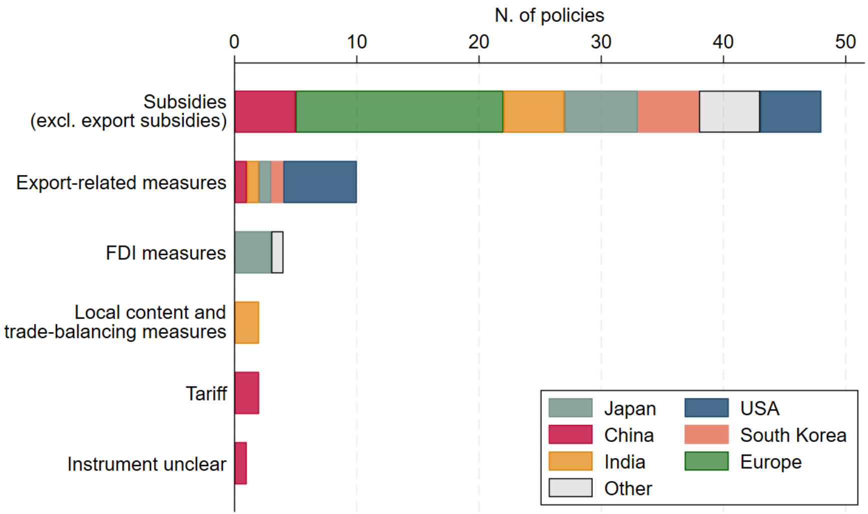
Governments target mainly Design and Manufacture

	All	National
i) Inputs	**18**	**9**
Semiconductor manufacturing equipment	13	8
Specialized chemicals and materials	8	6
Electronic Design Automation software	7	5
ii) Design and Manufacture	**35**	**22**
Integrated Device Manufacturers	23	15
Semiconductor designers	15	14
Foundries	21	16
iii) Assemble, Package, and Test	**10**	**9**
Too generic	10	10

Stated aims: growth, international competitiveness, and resilience

Goal	All	National
Economic growth and development	38	25
International competitiveness	23	14
Resilience	10	8
National security	6	5
Green economy	4	3
COVID-19 support	3	3
No goal available	1	1

Types of support – MAST classification



Quality Index

Return

1. **Residual variation of metal layers and polysilicon layers**
   $metal_{ijkt},\ poly_{ijkt} \quad \Rightarrow \quad \hat{u}^L_{ijkt}, \hat{u}^P_{ijkt}$

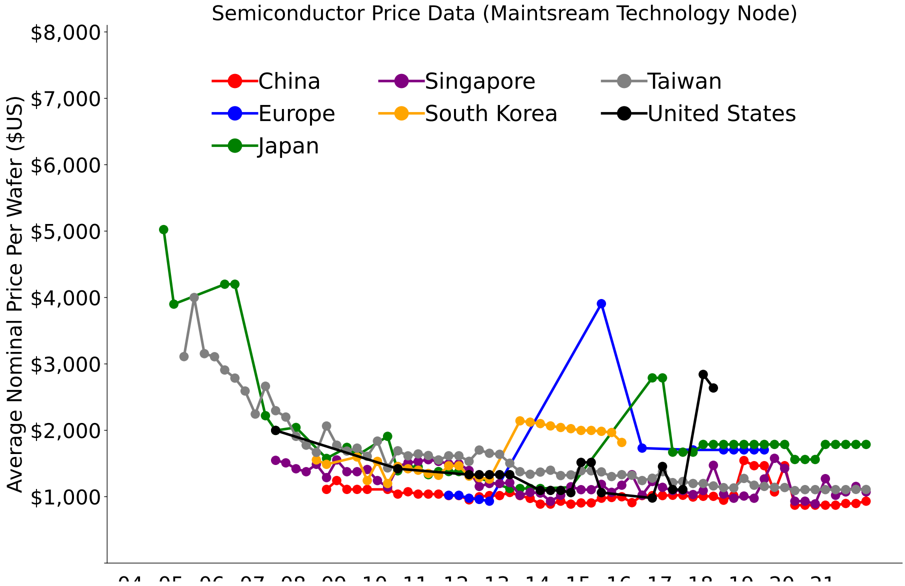
2. **Regression**
   $\log Q_{ijkt} = \beta_P \log P_{ijkt} + \gamma_m \tilde{m}_{ijkt} + \gamma_L \hat{u}^L_{ijkt} + \gamma_P \hat{u}^P_{ijkt} + \text{FE} + e_{ijkt}$

3. **Transaction-level quality**
   $\bar{z}_{ijkt} = \hat{\gamma}_m \tilde{m}_{ijkt} + \hat{\gamma}_L \hat{u}^L_{ijkt} + \hat{\gamma}_P \hat{u}^P_{ijkt}$

4. **Quality Index**
   $\bar{z}_{jkt} = \sum_i \log Q_{ijkt} \cdot \bar{z}_{ijkt}$

Price Trends for Mainstream Technology

Return



Yields

Return

- Contract manufacturing service providers typically assume the risk of product defects.
- If some products are defective, supplier must compensate by producing extra units to meet order requirements for functional products.
- This process increases the supplier's costs but does not generally affect the perceived product quality.

Yields

Return

- Our data contain yield information for 2005 through 2008 where survey respondents (buyers) report whether their order fell into one of four buckets: 0-25%, 26-50%, 51-75%, and 76-100%.

Table: Semiconductor Yields (2005-2008)

Country	0%-25%	26%-50%	51%-75%	76%-100%
China	0	0	0	100
Europe	0	0	0.72	99.27
Japan	0	1.8	4.5	93.69
Malaysia	0	0	0	100
Other	0	0	16	84
Singapore	0	0	3.87	96.12
South Korea	0	0	3.9	96.09
Taiwan	0.03	1.14	10.23	88.58
United States	0	7.88	14.1	78

Yields

Return

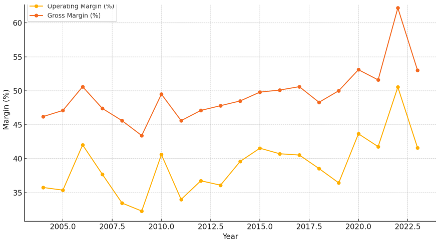
- In 2011-2012, GSA asked survey respondents to report exact yields.

Table: Yield Regression Results (2011-2012)

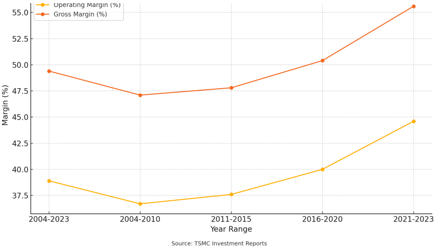
	Yield		Yield Reported	
Variable	Estimate	SE	Estimate	SE
China	0.0097	(0.0089)	0.1839	(0.0215)
Japan	-0.0035	(0.0292)	-0.2049	(0.0945)
Malaysia	-0.0104	(0.0172)	0.1502	(0.0649)
Singapore	0.0038	(0.0096)	-0.1000	(0.0875)
South Korea	-0.0151	(0.0141)	0.0175	(0.1208)
Europe	-0.0799	(0.0411)	-0.0524	(0.1287)
Other	-0.0610	(0.0048)	0.0885	(0.1352)
United States	-0.0606	(0.0642)	0.0220	(0.0726)
Metal Layers	-0.0137	(0.0075)	0.0006	(0.0153)
Number of Masks	0.0000	(0.0002)	0.0087	(0.0011)
Poly Layers	-0.0405	(0.0255)	-0.0319	(0.0512)
Quantity (Log)	0.0043	(0.0024)	-0.0079	(0.0088)
R^2	0.1605		0.1429	

TSMC Profit Margins

◂ Return



(a) By Year



(b) By Year Range